IN THE CLAIMS:

Set forth below in ascending order, with status identifiers, is a complete listing of all claims currently under examination. Changes to any amended claims are indicated by strikethrough and underlining. This listing also reflects any cancellation and/or addition of claims.

Claims 1-9 (cancelled)

Claim 10 (currently amended) A tracing system, comprising:

an embedded processor, said embedded processor including,

a processor core for executing instructions; and

trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced;

wherein said embedded processor further includes a trace memory and said tracing system is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints.

Claim 11 (original) The tracing system of claim 10, wherein said embedded processor further includes a trace capture block that receives trace data from said trace generation logic.

Claim 12 (original) The tracing system of claim 11, wherein said trace capture block sends trace data to an off-chip trace memory.

Claim 13 (original) The tracing system of claim 11, wherein said hardware input signals are received by said trace generation logic from said trace capture block.

Claim 14 (cancelled)

Claim 15 (original) The tracing system of claim 10, wherein said software-settable trace control register includes a trace select field that indicates whether said trace generation logic operates based on controls provided by said hardware input signals or by said software-settable trace control register.

Claim 16 (original) The tracing system of claim 10, wherein said software-settable trace control register is set by trace control commands that are embodied in one or more instructions of a program.

Claim 17 (original) The tracing system of claim 16, wherein said trace control commands are included within said program prior to execution of said program.

Claims 18-21 (cancelled)

Claim 22 (new) A tracing system, comprising:

an embedded processor, said embedded processor including,

a processor core for executing instructions; and

trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced;

wherein said tracing system is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints and said software-settable trace control register includes a trace select field that indicates whether said trace generation logic operates based on controls provided by said hardware input signals or by said software-settable trace control register.

Claim 23 (new) The tracing system of claim 22, wherein said embedded processor further includes a trace capture block that receives trace data from said trace generation logic.

Claim 24 (new) The tracing system of claim 22, wherein said trace capture block sends trace data to an off-chip trace memory.

Claim 25 (new) The tracing system of claim 22, wherein said hardware input signals are received by said trace generation logic from said trace capture block.

Claim 26 (new) The tracing system of claim 22, wherein said embedded processor further includes a trace memory.

Claim 27 (new) The tracing system of claim 22, wherein said software-settable trace control register is set by trace control commands that are embodied in one or more instructions of a program.

Claim 28 (new) The tracing system of claim 27, wherein said trace control commands are included within said program prior to execution of said program.